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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/270,256	03/15/1999	ILYA KLEBANOV	0100.9900440	2265

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EXAMINER	
YANG, RYAN R	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/270,256	KLEBANOV, ILYA	
	Examiner	Art Unit	
	Ryan R. Yang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6-11,13,17,18 and 21-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6-11,13,17,18 and 21-33* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/13/2006 has been entered.

2. This action is responsive to communications: Amendment, filed on 2/13/2006. This action is non-final.

3. Claims 2, 6-11, 13, 17-18 and 21-33 are pending in this application. Claims 21-23 are independent claims.

4. The present title of the invention is "Method and Apparatus for Rendering an Image in a Video Graphics Adapter" as filed originally.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 21, 2, 8-11, 23, 24-28 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (5,959,639) and further in view of Reddy (5,712,664).

As per claim 21, Wada discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 11, item 9a is VGA receives a first frame of video);

rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal, wherein the first control signal is a signal specifying a window location for displaying the active video (Figure 11, 12a is one video segment correspond to 9a);

storing at least a first portion of the active video in a video memory associated with the first VGA (Figure 11, item 1 main memory is associated with 9a); and

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal (Figure 11, 12b is one video segment correspond to 9b) and storing at least second portion of the active decoded video in the memory associated with the first VGA (Figure 11, item 1 main memory is associated with 9a).

Wada discloses a method of displaying active video. It is noted that Wada does not explicitly disclose where the memory association is specifically accomplished by mapping. However, this is known in the art as taught by Reddy. Reddy discloses a shared memory graphics accelerator system in which a portion of memory location is mapped to the first VGA (Figure 3 and "one integrated graphics display memory elements works on even lines of the CRT display while the other integrated graphics display memory element is drawing odd lines on the CRT screen 310", column 4, line 35-67, wherein the IGDM is considered a VGA, DRAM is considered a memory and the even and odd lines are considered location specific portions).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teach of Reddy into Wada because Wada discloses a method of displaying an active video and Reddy discloses the video data could be distributed in order increase the system performance.

7. As per claim 23, Wada discloses an active video processing system comprising:

a first video graphics adapter (VGA) operative to receive a first frame of active video data, and in response display at least a first portion of the first frame of active video data at a window location in response to a first control signal (Figure 11, item 9a is VGA receives a first portion of first frame of video);

a first video memory operatively coupled to the first VGA and operative to store at least the first portion of the active video data (Figure 11, item 1 main memory is associated with 9a);

a second VGA, operatively coupled to the first VGA and operative to receive the at least a second portion of the first frame of active video data, and in response to display at least the second portion of the first frame of active video data (Figure 11, item 9b is VGA receives a second portion of first frame of video); and

a second video memory operatively coupled to the second VGA and operative to store at least the second portion of the active video data (Figure 11, item 1 main memory is associated with 9b).

Wada discloses a method of displaying active video. It is noted that Wada does not explicitly disclose where the memory association is specifically accomplished by mapping. However, this is known in the art as taught by Reddy. Reddy discloses a

shared memory graphics accelerator system in which a portion of memory location is mapped to the first VGA (Figure 3 and "one integrated graphics display memory elements works on even lines of the CRT display while the other integrated graphics display memory element is drawing odd lines on the CRT screen 310", column 4, line 35-67, wherein the IGDM is considered a VGA, DRAM is considered a memory and the even and odd lines are considered location specific portions).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teach of Reddy into Wada because Wada discloses a method of displaying an active video and Reddy discloses the video data could be distributed in order increase the system performance.

8. As per claims 8 and 31, Wada and Reddy demonstrated all the elements as applied to the rejected claims 21 and 23, supra, respectively, and Wada further discloses the first VGA is a primary VGA (where Figure 11 Graphics Controller 9a is considered primary), and the second VGA is a secondary VGA (where Figure 11 Graphics Controller 9b is considered secondary).

9. As per claims 9 and 32, Wada and Reddy demonstrated all the elements as applied to the rejected claims 21 and 23, supra, respectively, and Wada further discloses the first VGA is a secondary VGA (where Figure 11 Graphics Controller 9a is considered secondary), and the second VGA is a primary VGA (where Figure 11 Graphic Controller 9b is considered primary).

10. As per claims 10 and 33, Wada and Reddy demonstrated all the elements as applied to the rejected claims 21 and 23, supra, respectively, and Wada further

discloses the first VGA and the second VGA are part of a video wall such that the first frame of active video is displayed across multiple displays simultaneously (Figure 11, where 12a-12d are considered multiple displays).

11. As per claim 11, Wada and Reddy demonstrated all the elements as applied to the rejected claim 21, and Reddy further discloses receiving at the second VGA a second frame of active video from a second video source (Figure 4 when the external memory is added to each VGA and each external memory is considered a video source, column 5, line 24-24); and

rendering at least a portion of the second frame of video at the first VGA (since the video data could be redistributed among the DRAM, column 4, line 49-54).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teach of Reddy into Wada because Wada discloses a method of displaying an active video and Reddy discloses the video data could be distributed in order increase the system performance.

12. As per claim 25, Wada and Reddy demonstrated all the elements as applied to the rejection of independent claim 23, supra, and Wada further discloses the first VGA further includes a video graphics processor (Figure 11, item 6a), and the second VGA further includes a video graphics processor (Figure 11, item 6b).

13. As per claim 26, Wada and Reddy demonstrated all the elements as applied to the rejection of independent claim 23, supra, and Wada further discloses the window operates in conjunction with an operating system, such that the operating system

supports the display of the active video data on the first VGA (Figure 11, item 17a is a operating system).

14. As per claim 27, Wada and Reddy demonstrated all the elements as applied to the rejection of independent claim 23, supra, and Wada further discloses the window operates in conjunction with an operating system, such that the operating system supports a program for providing the active video data only to the first VGA (Figure 11, items 6a supports a program).

15. As per claims 2 and 28, Wada and Reddy demonstrated all the elements as applied to the rejection of independent claims 21 and 23, supra, respectively, and Wada further discloses the first portion and the second portion are the same portion (when a portion is a frame).

16. As per claim 24, Wada and Reddy demonstrated all the elements as applied to the rejection of independent claim 23, and Reddy further discloses wherein the first VGA receives the first control signal when the first VGA receives a command to display at least the second portion of the first frame of active video data on the second VGA (since the image can be redistributed by a control signal, column 4, line 49-55).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teach of Reddy into Wada because Wada discloses a method of displaying an active video and Reddy discloses the video data could be distributed in order increase the system performance.

17. Claims 22 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knox et al. (6,323,854) and further in view of Reddy (5,712,664).

As per claim 22, Knox et al., hereinafter Knox, disclose a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 2, where item 200 is the first video adapter), wherein the video source is at least one of the following: a video decoder and television signal (Figure 2, the PCI bus input video data which includes TV signals); and

displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal (Figure 2, item 200 is the first video adapter and 102 is the second adapter; "secondary card 102 typically provides more sophisticated graphics, here accessing the video controller 100 through a PCI interface 128, column 3, line 7-9), wherein the second control signal is a signal specifying a window location for displaying the active video, ("referring to a single monitor 654 ... The CRTC/controller 220 can be instructed by the video controller 200 that it is only to display a particular portion of the image which is actually transmitted over the bus 210", column 9, line 18-24).

Knox discloses a method of displaying active video. It is noted that Knox does not explicitly disclose where the memory association is specifically accomplished by mapping. However, this is known in the art as taught by Reddy. Reddy discloses a shared memory graphics accelerator system in which a portion of memory location is mapped to the first VGA (Figure 3 and "one integrated graphics display memory elements works on even lines of the CRT display while the other integrated graphics display memory element is drawing odd lines on the CRT screen 310", column 4, line

35-67, wherein the IGDM is considered a VGA, DRAM is considered a memory and the even and odd lines are considered location specific portions).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teach of Reddy into Knox because Knox discloses a method of displaying an active video and Reddy discloses the video data could be distributed in order increase the system performance.

18. As per claim 17, Knox and Reddy demonstrated all the elements as applied to the rejection of independent claim 22, supra.

As for the video decoder is for decoding a compressed video signal, it is inherent that a video signal to be decoded is a compressed signal.

19. As per claim 18, Knox and Reddy demonstrated all the elements as applied to the rejection of independent claim 22, supra, and Reddy further discloses wherein the method further comprises the video source sending the first frame of data over a bus local to first VGA (Figure 4 where the external memory can be added and the external memory is considered the video source connected locally to each VGA, column 5, line 24-33).

20. Claims 6-7 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada and Reddy as applied to claim 21 above, and further in view of Dennison et al. (4,729,119).

21. As per claims 6 and 29, Wada and Reddy demonstrated all the elements as applied to the rejected claim 21, supra, respectively.

Wada and Reddy disclose a system of displaying video on multiple computer displays. It is noted that Wada and Reddy do not explicitly disclose the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the first VGA, however, this is known in the as taught by Dennison et al., hereinafter Dennison. Dennison discloses a memory system in which the central can be alternately used by a DMA (column 8, line 54-60).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Dennison into Wada and Reddy because Wada and Reddy disclose a method of displaying on a multi-display computer system and Dennison discloses the controller can be alternately used by a DMA in order to allow for faster access of the memory.

22. As per claims 7 and 30, Wada and Reddy demonstrated all the elements as applied to the rejected claim 21, supra, respectively.

Wada and Reddy disclose a system of displaying video on multiple computer displays. It is noted that Wada and Reddy do not explicitly disclose discloses the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the second VGA, however, this is known in the as taught by Dennison et al., hereinafter Dennison. Dennison discloses a memory system in which the central can be alternately used by a DMA (column 8, line 54-60).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Dennison into Wada and Reddy because Wada and Reddy disclose a method of displaying on a multi-display computer

system and Dennison discloses the controller can be alternately used by a DMA in order to allow for faster access of the memory.

23. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada and Reddy as applied to claim 21 above, and further in view of Lumelsky (4,949,169).

As per claim 13, Wada and Reddy demonstrated all the elements as applied to the rejected claim 21, supra.

Wada and Reddy disclose a system of displaying video on multiple computer displays. It is noted that Wada and Reddy do not explicitly disclose the step of storing the window location in a preference file, however, this is known in the art as taught by Lumelsky et al., hereinafter Lumelsky. Lumelsky discloses in a video-graphics display window environment in which the window location is stored in a preference file ("Vertical Sample Initial Address Register (SYA) 94 and Horizontal Sample Initial Address Register (SXA) 96. These two registers specify the destination window location. Two loadable counters, Vertical Sampling Address Counter (SYCNT) 98 and horizontal Sampling Address Counter (SXCNT) 100 are used as pointers to the receiving node's frame buffer (SYADDR and SXADDR)", column 14, line 30-37).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lumelsky into Wada and Reddy because Wada and Reddy disclose a method of displaying video data on multiple display and Lumelsky discloses a method of tacking the window location in order to correctly display the window on different displays.

Response to Arguments

24. Applicant's arguments with respect to claims 11, 18 and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inquiries

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan R. Yang whose telephone number is (571) 272-7666. The examiner can normally be reached on M-F 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Yang
Primary Examiner
May 1, 2006